AMENDMENTS TO THE SPECIFICATION

Page 9, eighth full paragraph:

Fig. 8 is an enlarged sectional view for schematically showing a structure of a part of the semiconductor device according to a variation of the second embodiment of the present invention.

Page 16, between paragraph 1 and 2 insert the following:

Electrode pads 2a and 2b are also shown in Fig. 5.

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (Currently Amended) A semiconductor device comprising:

a first semiconductor chip which has a first surface;

an external connecting terminal which is formed on said first surface ~~and which has~~, said external connecting terminal having a primary height with respect to said first surface;

a second semiconductor chip which is mounted on said first surface ~~through a bump and which has~~,

wherein said second semiconductor chip has a secondary height with respect to said first surface; and

said secondary height is smaller than said primary height.

2. (Currently Amended) A semiconductor device comprising:

a first semiconductor chip which has a first surface;

an external connecting terminal which is formed on said first surface ~~and which has~~, said external connecting terminal having a primary height with respect to said first surface;

a second semiconductor chip which is mounted on said first surface ~~through a bump and which has~~, said second semiconductor chip having a secondary height with respect to said first surface; and

a rewiring which electrically connects said first semiconductor chip, said second semiconductor chip, and said external connecting terminal with each other and which is located on said first surface ~~; and~~,

wherein said second semiconductor chip ~~being processed~~ is thin ~~so that~~ whereby said secondary height ~~being~~ is smaller than said primary height.

3. (Currently Amended) A semiconductor device comprising:

a first semiconductor chip which has a first surface;

an external connecting terminal which is formed on said first surface ~~and which has~~, said external connecting terminal having a primary height with respect to said first surface;

a second semiconductor chip which is mounted on said first surface through a bump ~~and which has~~, said second semiconductor chip having a secondary height with respect to said first surface;

a rewiring which electrically connects said first semiconductor chip, said second semiconductor chip, and said external connecting terminal with each other and which is located on said first surface;

an insulating layer which is overlaid on said rewiring and which has predetermined opening portions in a first region for forming said external connecting terminal and in a second region for mounting said second semiconductor chip, respectively; and

bedding electrodes which are formed in said predetermined opening portions respectively, said external connecting terminal ~~being consisting of~~ comprising BGA and being

positioned on said bedding electrode in said first region, said second semiconductor chip being flip chip bonded to said bedding electrode in said second region through said bump ~~; and,~~

wherein said second semiconductor chip ~~being processed~~ is thin ~~so that~~ whereby said secondary height ~~being~~ is smaller than said primary height.

4. (Original) A semiconductor device as claimed in claim 3, wherein said insulating layer is made of at least two resins of which elastic characteristics are different from each other, one resin being in said first region while another resin being in said second region.

5. (Original) A semiconductor device as claimed in claim 3, wherein both said bedding electrode in said first region and said bedding electrode in said second region are made of the same material provided in the same process.

6. (Original) A semiconductor device as claimed in claim 4, wherein both said bedding electrode in said first region and said bedding electrode in said second region are made of the same material provided in the same process.

7. (Original) A semiconductor device as claimed in claim 3, wherein said bedding electrode in said first region and said bedding electrode in said second region are made of different materials from each other.

8. (Original) A semiconductor device as claimed in claim 4, wherein said bedding electrode in said first region and said bedding electrode in said second region are made of different materials from each other.

9. (Original) A semiconductor device as claimed in claim 6, wherein a film including a material different from that of said bedding electrode is stacked on said bedding electrode.

10. (Original) A semiconductor device as claimed in claim 8, wherein a film including a material different from that of said bedding electrode is stacked on said bedding electrode.

11. (Original) A semiconductor device as claimed in claim 1, wherein said second semiconductor chip further comprises a projection on another surface thereof opposite to a junction surface mounted to said first semiconductor chip, said projection having a ternary height with respect to said another surface of said second semiconductor chip; and said ternary height being determined so that said primary height being substantially equal to the sum of said secondary height and said ternary height.

12. (Original) A semiconductor device as claimed in claim 11, wherein said projection is made of a material selected from the group consisting of metal, conductive resin, and insulating resin.

13. (Original) A semiconductor device as claimed in claim 11, wherein said junction surface of said second semiconductor chip mounted to said first semiconductor chip through said bump is sealed by resin.

14. (Original) A semiconductor device as claimed in claim 3, further comprising a resin layer which is provided on said bedding electrode in said first region and which includes via hole penetrating to the bedding electrode in said first region, and a conductor which is buried into said via hole and which electrically connects said external connecting terminal with the bedding electrode in said first region.

15. (Original) A semiconductor device as claimed in claim 1, wherein said first semiconductor chip comprises a member selected from the group consisting of a semiconductor chip, a function device, and an electronic component.

16. (Original) A semiconductor device as claimed in claim 1, wherein said second semiconductor chip comprises a member selected from the group consisting of a semiconductor chip, a function device, and an electronic component.

17. (Currently Amended) A semiconductor device as claimed in claim 1, wherein said second semiconductor chip ~~comprises~~ is constituted by a plurality of chips combining a member selected from ~~the~~ a group ~~consisting of~~ comprising a semiconductor chip, a function device, and an electronic component.

18. (Original) A semiconductor device as claimed in claim 1, wherein said second semiconductor chip is processed thin by the use of at least one method selected from the group consisting of grinding, polishing, wet etching and dry etching.

19 – 25 (Canceled).

26 (New): A semiconductor device as claimed in claim 1, wherein said external connecting terminal comprises BGA.

27 (New): A semiconductor device as claimed in claim 1, wherein said second semiconductor chip is connected to said first semiconductor chip through a bump.

28 (New): A semiconductor device as claimed in claim 2, wherein said external connecting terminal comprises BGA.

29 (New): A semiconductor device as claimed in claim 2, wherein said second semiconductor chip is connected to said first semiconductor chip through a bump.

AMENDMENTS TO THE DRAWINGS

Attachment: Replacement Drawing Sheet – Fig. 8

REMARKS

Applicant cancels claims 19-25 without prejudice or disclaimer, and adds new claims 26-29. Therefore, claims 1-18 and 26-29 are now pending in this application.

Applicant amends independent claims 1-3 and dependent claim 17 more clearly to recite the features of the embodiments defined therein. These amendments do not narrow the scope of the original claims 1-3 and 17, but are merely for clarification purposes. No estoppel is created.

Also, Applicant adds new dependent claims 26-29 more fully to cover various aspects of the embodiments of the invention as described in the claims.

The Examiner rejects:

- claims 1-18 under 35 U.S.C. §112, second paragraph, due to allegedly unclear recitation in independent claims 1-3 and claim 17; and
- claims 1, 2 and 15-18 under 35 U.S.C. §102(e) as being anticipated by a Shiraishi et al. (Shiraishi).

Also, the Examiner objects to the drawings and the specification for the reasons set forth on page 2 of the Office Action.

The Examiner indicates that claims 3-14 would be **allowable** if rewritten to overcome the §112, second paragraph, rejection, and as far as claims 12 and 13 are concerned to include all of the limitations of the base claim and any intervening claims.

With regard to the §112, second paragraph, rejection, the claims as amended above are in full compliance with the requirements of §112, second paragraph. Thus, this rejection should be withdrawn. Accordingly, claims 3-11 and 14 should be in condition for immediate allowance.

With regard to the Examiner's objections to the drawings and the specification, these objections are address by the amendments to the specification as set forth above, and by the Replacement drawing sheet (Fig. 8) submitted herewith. Also, with regard to the Examiner's objections to the informalities in the drawing figures filed December 3, 2001, Applicant respectfully submits that these informalities have been addressed and overcome by the Formal Drawings filed February 15, 2002. The Examiner is respectfully requested to confirm the receipt of and approve these formal drawings (together with the Replacement Drawing Sheet – Fig. 8 submitted herewith).

With regard to the Examiner's prior art rejection, Applicant respectfully traverses this rejection as follows.

Applicant's inventions as defined in independent claims 1 and 2 provides a semiconductor device comprising a unique combination of features, including *inter alia*:

> a first semiconductor chip which has a first surface;
>
> an external connecting terminal which is formed on said first surface, said external connecting terminal having a primary height with respect to said first surface;
>
> a second semiconductor chip which is mounted on said first surface,
>
> wherein said second semiconductor chip has a secondary height with respect to said first surface; and
>
> said secondary height is smaller than said primary height (claim 1; see also claim 2).

An example of the semiconductor device as defined in claim 1 is illustrated in Applicant's Fig. 5 (see also Applicant's specification at page 16, lines 4-24).

Shiraishi discloses a module which has a first semiconductor element 101 and a second semiconductor element 301. Shiraishi further discloses that the second semiconductor element 301 "can be larger than" the first semiconductor element 101, and that the first element 101 is mounted on a multilayer wiring board 107 using "junctions 110". Nowhere does Shiraishi describe the relative height of either of its semiconductor elements 101, or 301, with respect to the height of an external connecting terminal of the corresponding other element. Thus, Shiraishi does not disclose, and is incapable of suggesting a semiconductor device wherein the height of an external connecting terminal with respect to a surface of a first semiconductor chip is greater than a height of a second semiconductor chip (mounted on the surface of the first semiconductor chip) with respect to the surface of the first semiconductor chip, as required by Applicant's claims 1 and 2.

Furthermore, with regard to Applicant's independent claim 2, a rewiring which electrically connects a first semiconductor chip, a second semiconductor chip, and an external connecting terminal with each other, is located on a surface of the first semiconductor chip. On the other hand, Shiraishi discloses an external terminal (for connecting the semiconductor device to the outside) which is mounted on a second chip. As a result, in Shiraishi, the external terminal is positioned at the outer peripheral portion of the second chip, and it is necessary to prepare the wiring layer larger than the chip sizes of the first and second chips. In contradistinction to Shiraishi, according to Applicant's invention as claimed in claim 2 not only the electrode for connecting the first chip and the second chip, but also the electrode for connecting the semiconductor device to the outside are included within the principal surface of the first chip.

Further, when a wiring layer such as that of Shiraishi is used, the wiring layer and the first chip, the wiring layer and the second chip must be connected by the bumps, respectively. This inevitably increases the cost of production.

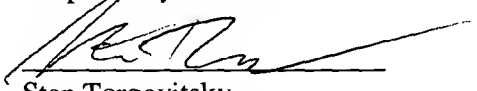
One of the benefits which maybe achieved by the embodiments of Applicant's invention as claimed in claims 1 and 2, is that a size of a semiconductor package is essentially the size of the first chip.

Accordingly, Applicant's independent claims 1 and 2, as well as the dependent claims 15-18 (which incorporate all the novel and unobvious features of their base claim 1) are not anticipated by (i.e., are not readable on) Shiraishi at least for this reason.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned attorney at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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